Fig.1 (Prior Art)

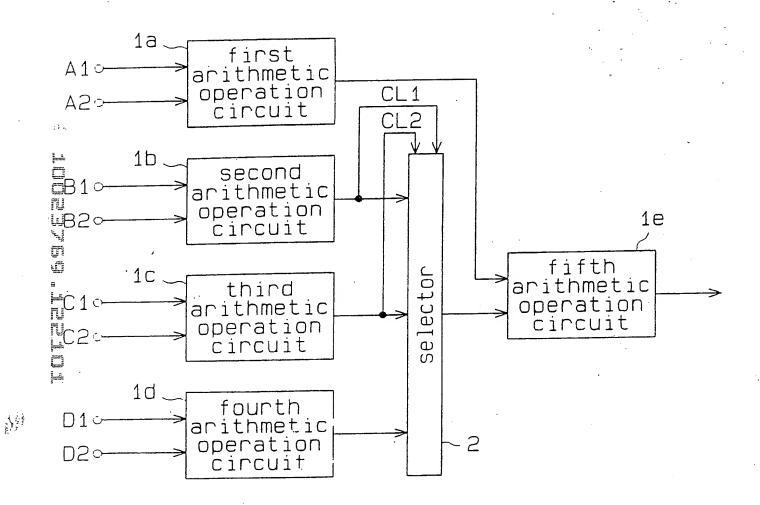
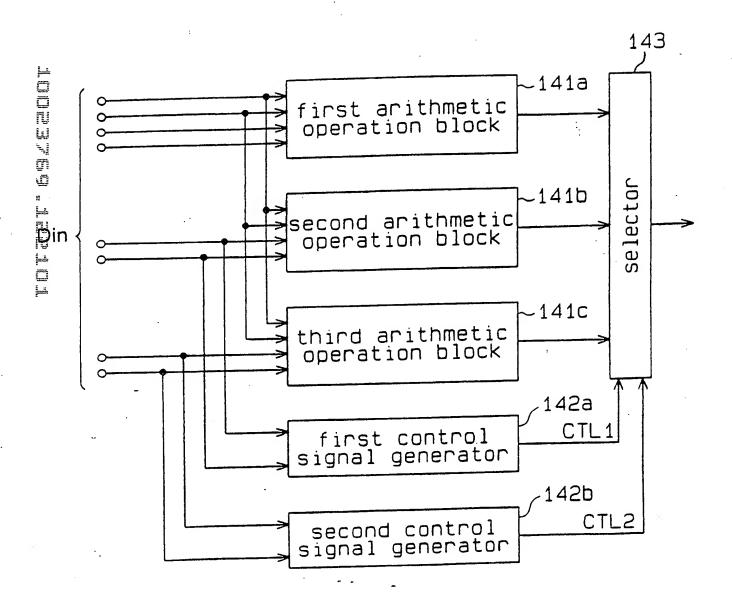


Fig.2



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Fig.3

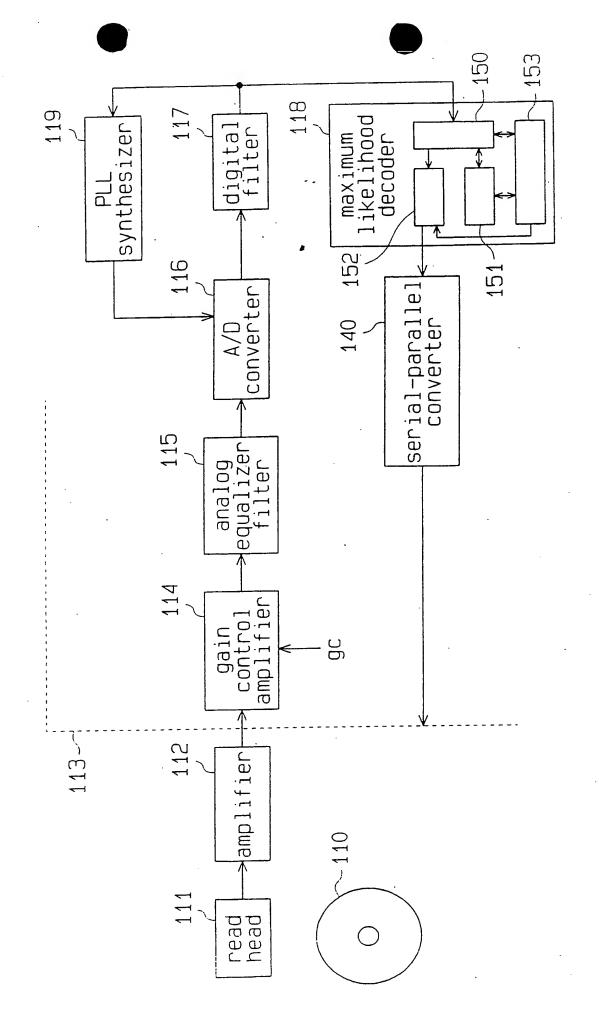
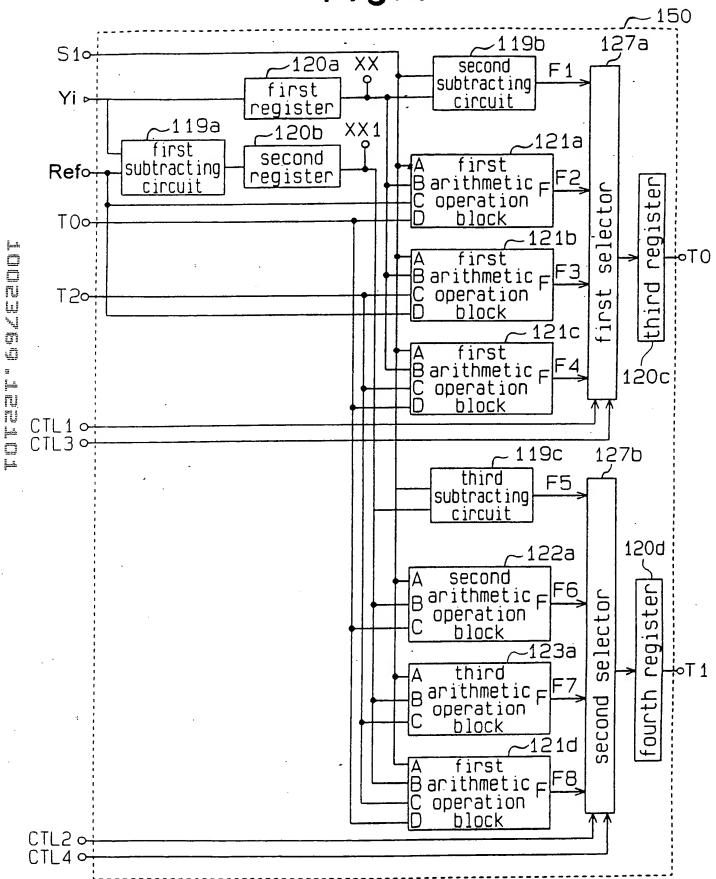
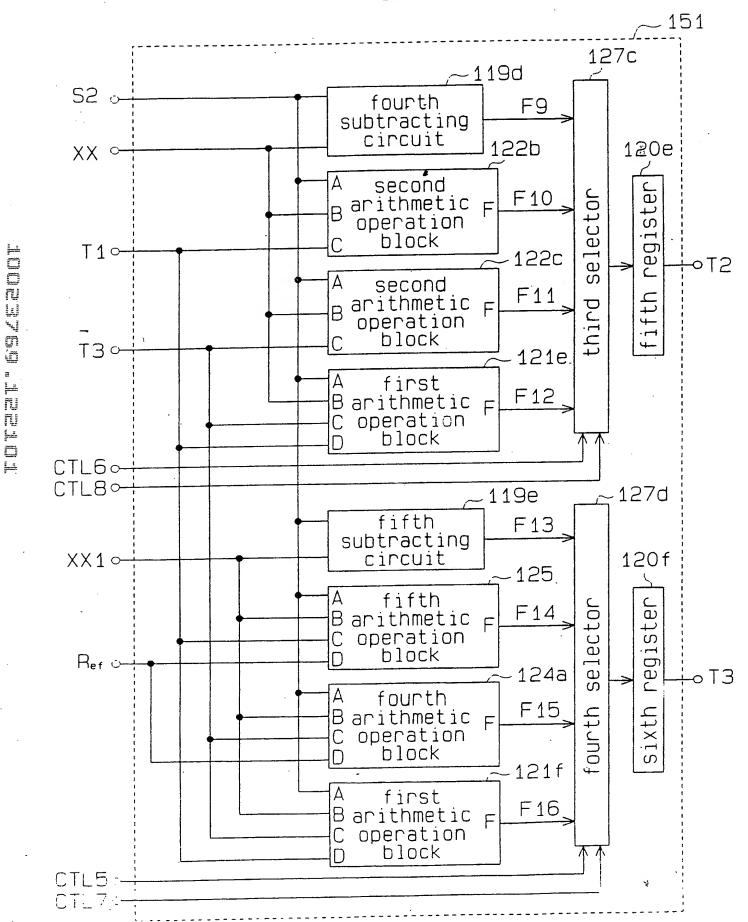


Fig.4



17.79

Fig.5



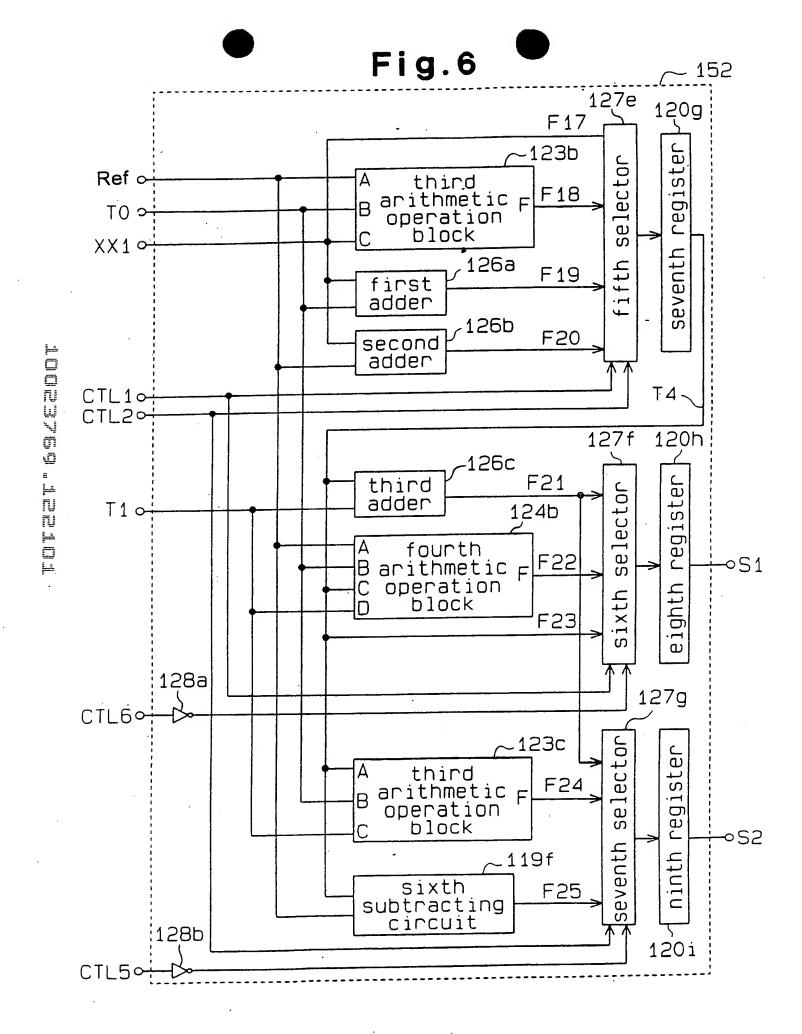


Fig.7

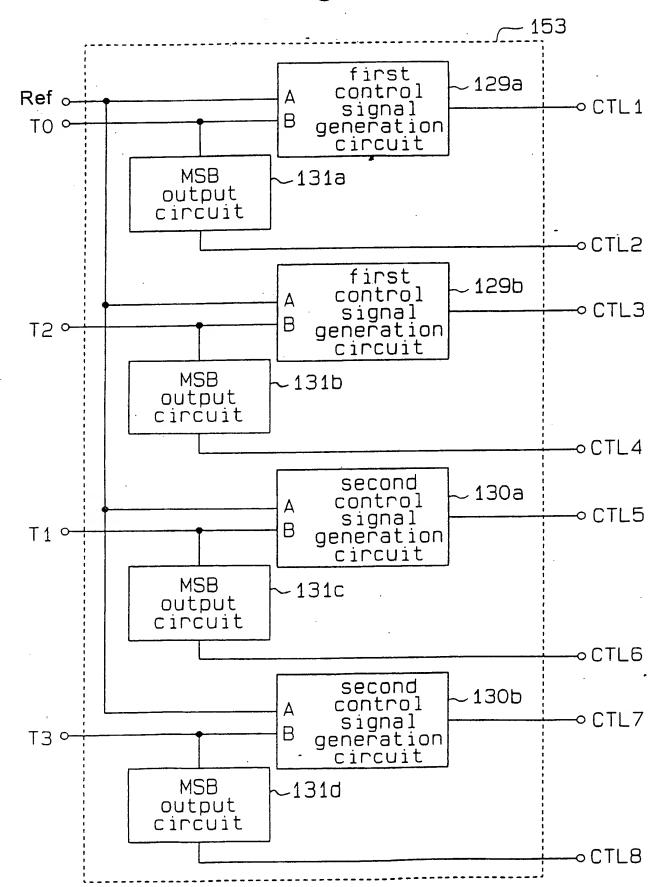
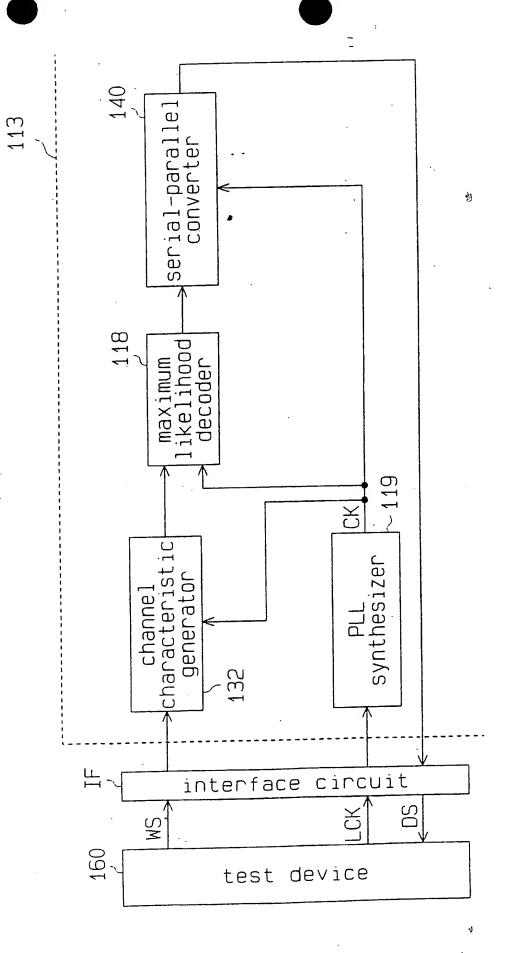


Fig.8



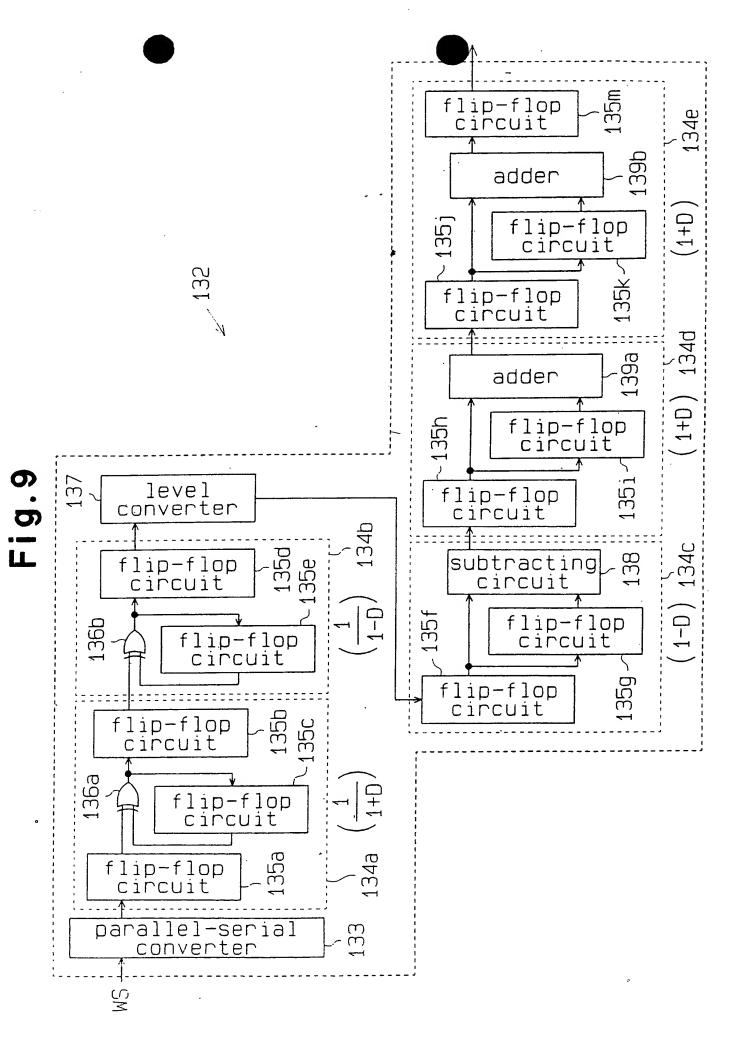
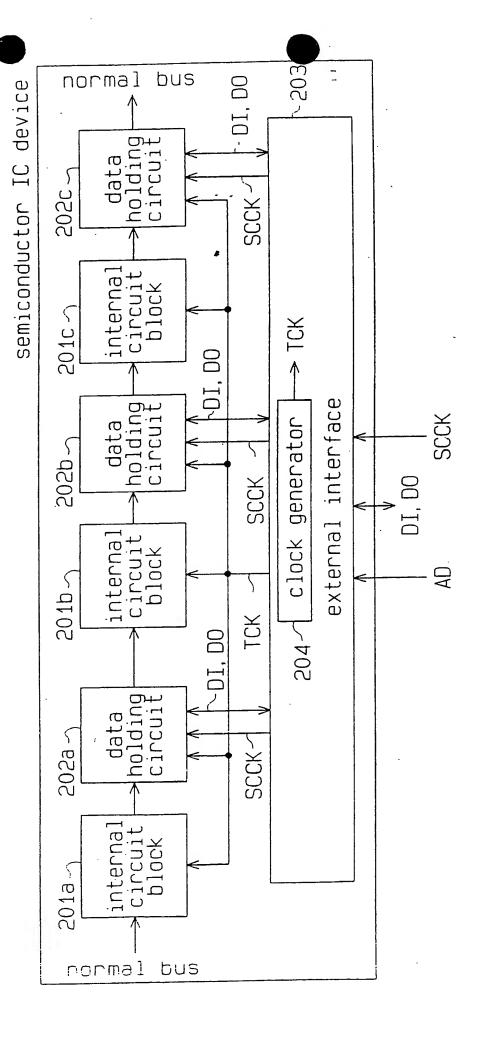
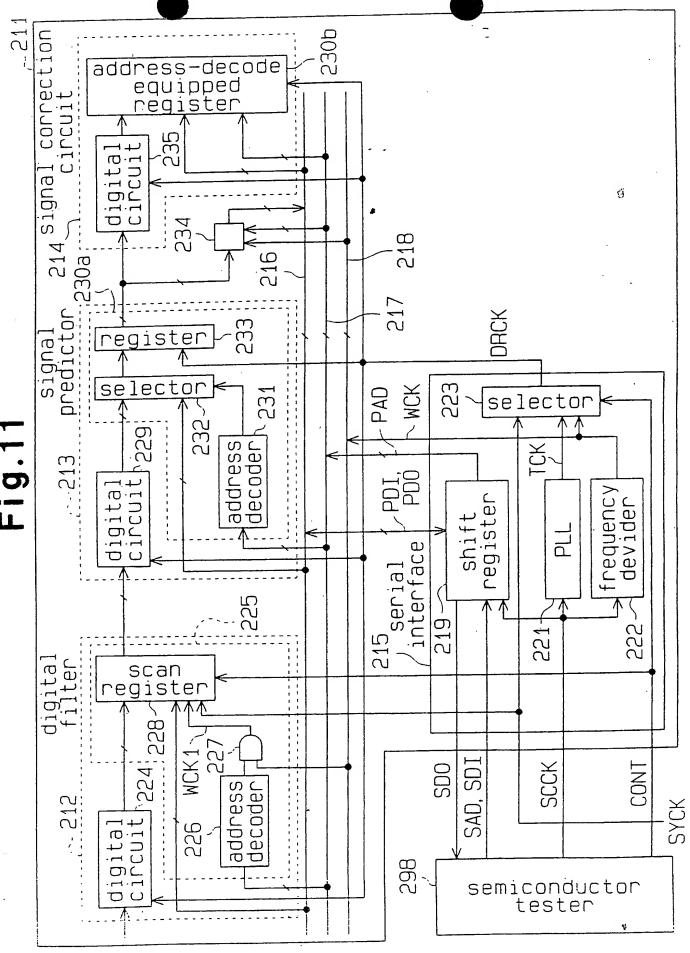


Fig.10

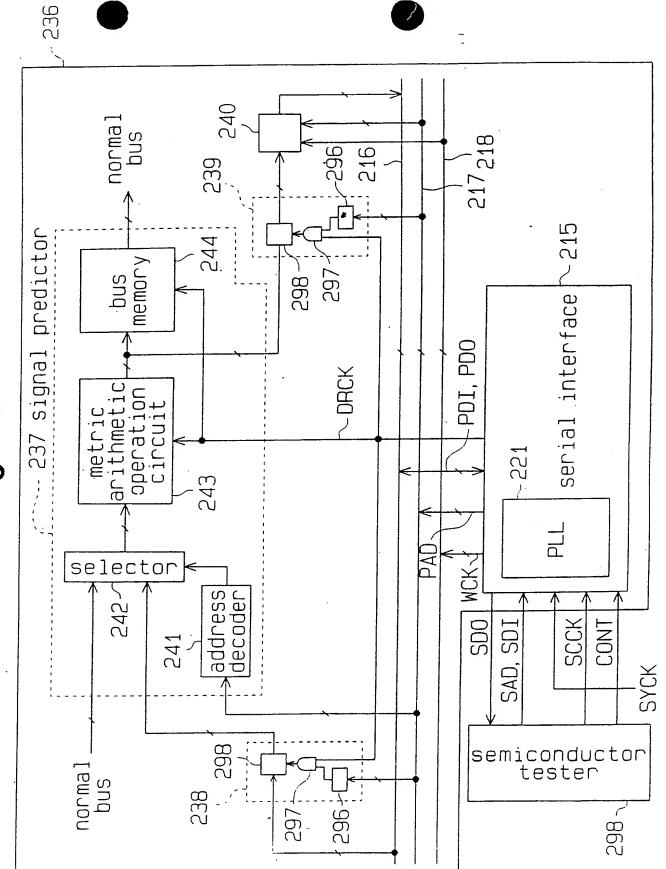
<u>:</u>.





12.2

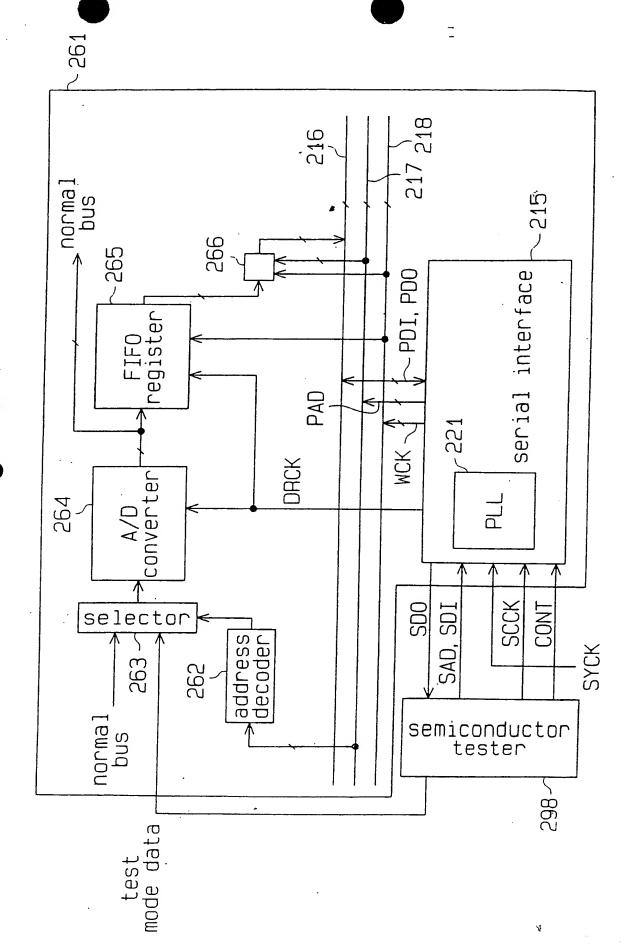
Fig.12

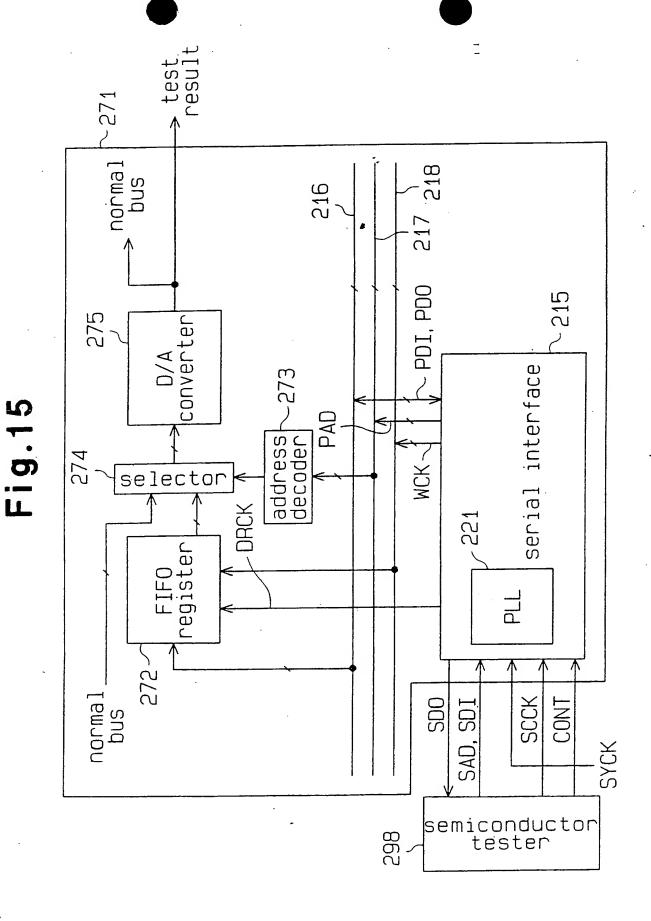


245 218 248 216 215 257 interface PDI, ~ 247 ~246 serial .221 FIF0 register 252 256 FIFO register WCK DRCK PAD H selector 2557 selector SCCK SDO CONT SOI 251. 253 selector SAD, selector address address 249 250 254 semiconductor tester

 $\int_{M} h(\hat{x}) d\hat{x} = 1$

Fig.14

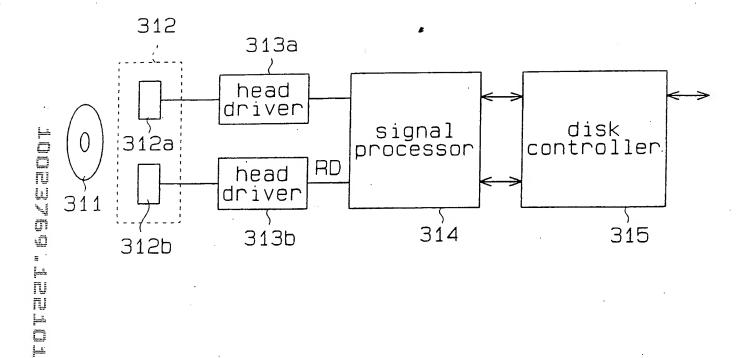




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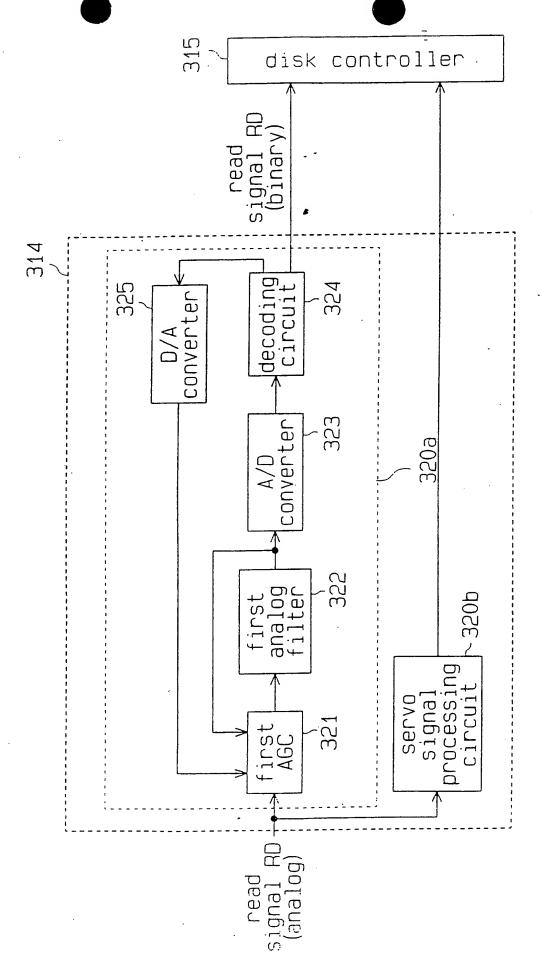
normal bus 295 218 ø 216 294 286 register selector 2937 address selector ⇒normaj bus normal bus > 215 DRCK 292, Fig.17 291 serial interface 290 register 289. 221 address selector FIFO 2887 밀 287 PAD, SDO SCCK CONT normal> bus SAD, SYCK semiconductor tester 298

Fig.18



M





RST STR VB STD STC STB STA* 335 343 track hold circuit 3 disk controller counter 315~ AL CHG 345 346 CHS 348 reference voltage generator 345 conversion amplifier voltage -current ~320b 쏫 1 334 344 zero-cross detector 333 wave 341 peak detector 332 second analog filter 336~ 331 second AGC read signal RD (analog ¥

Fig. 21

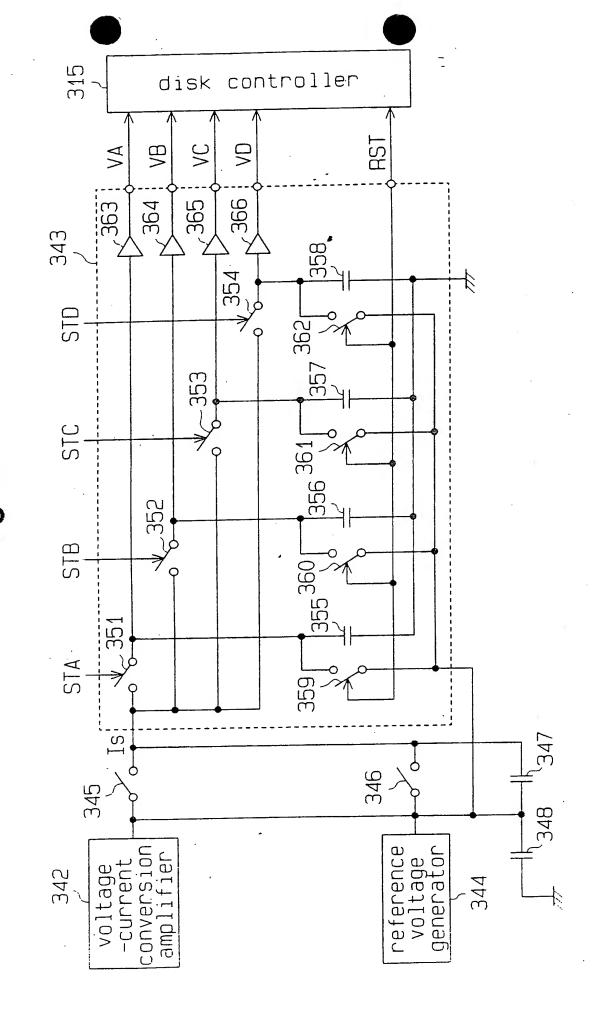
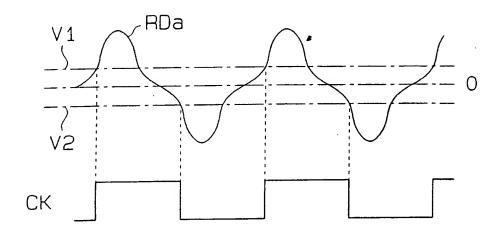
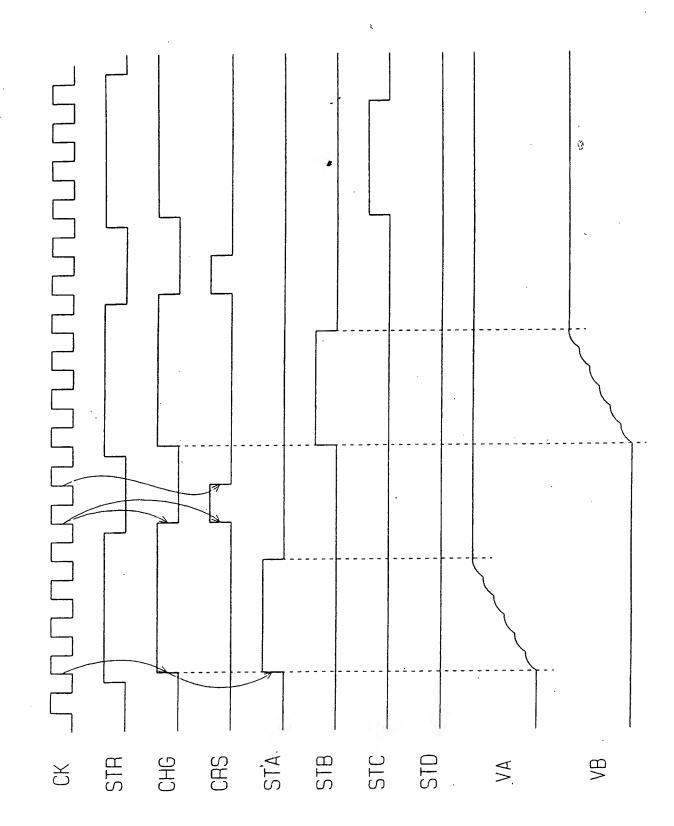


Fig. 22





rorettescriot Fig.24

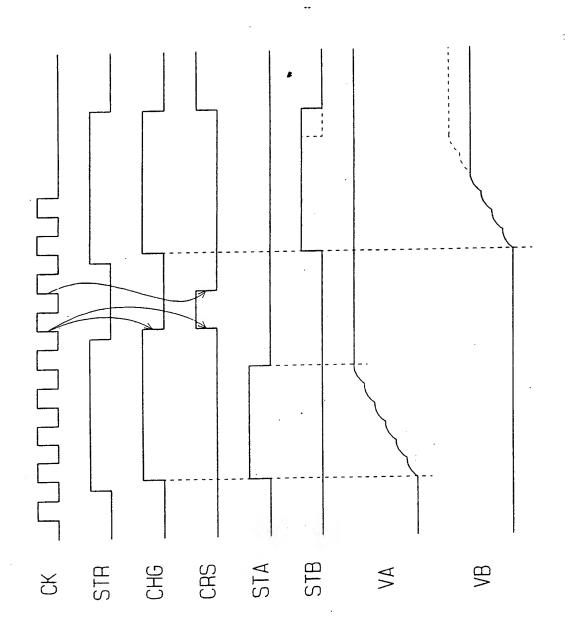


Fig. 25

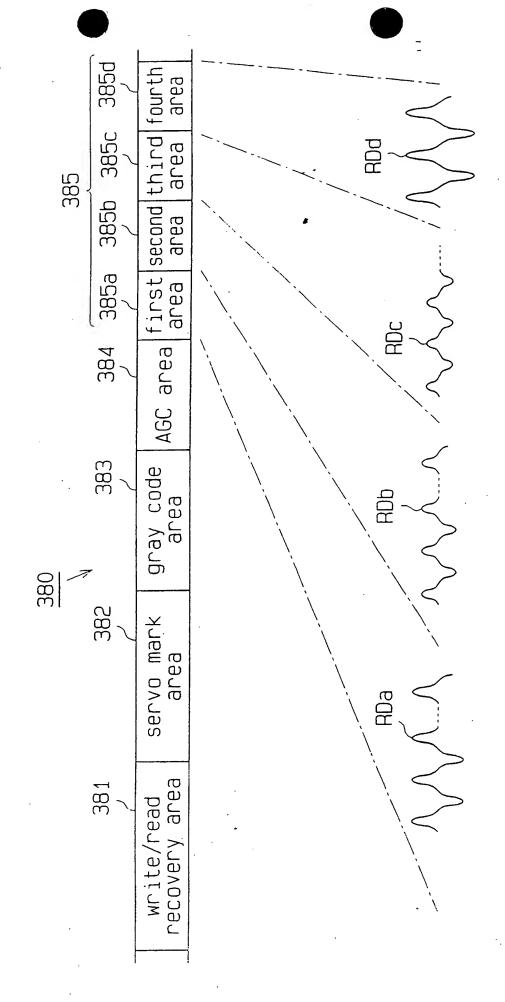
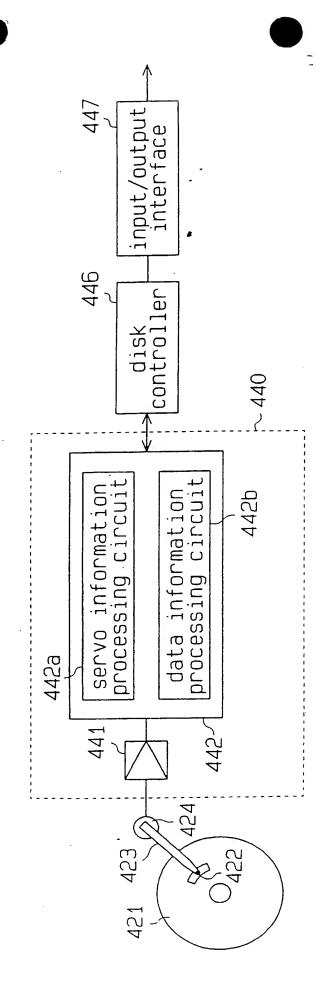
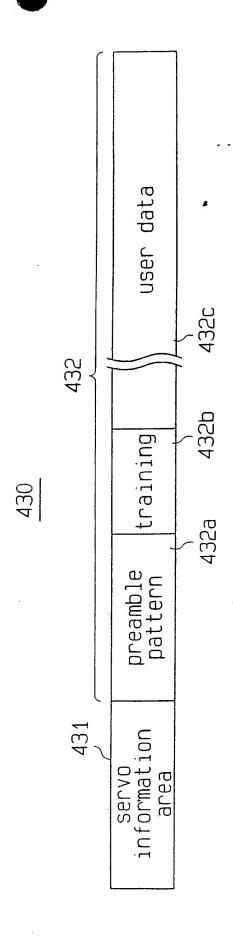


Fig.26



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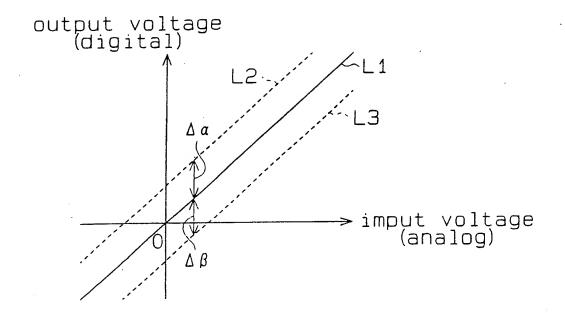
Fig. 27



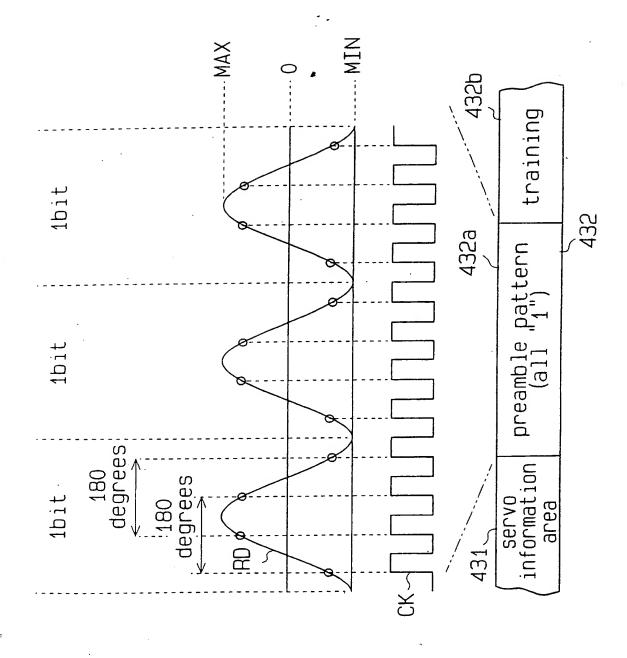
446 controllêr disk 442b serial interface ~ 451 discriminator 꼿 first register 456 452-FIG 28 multiplier 454 control circuit SB Ja 453 __ 무. 445 b gain control amplifier 443 9 adder 455 エ selector 462 463 ×~461 458 460 444 second register D/A 459 450 \perp

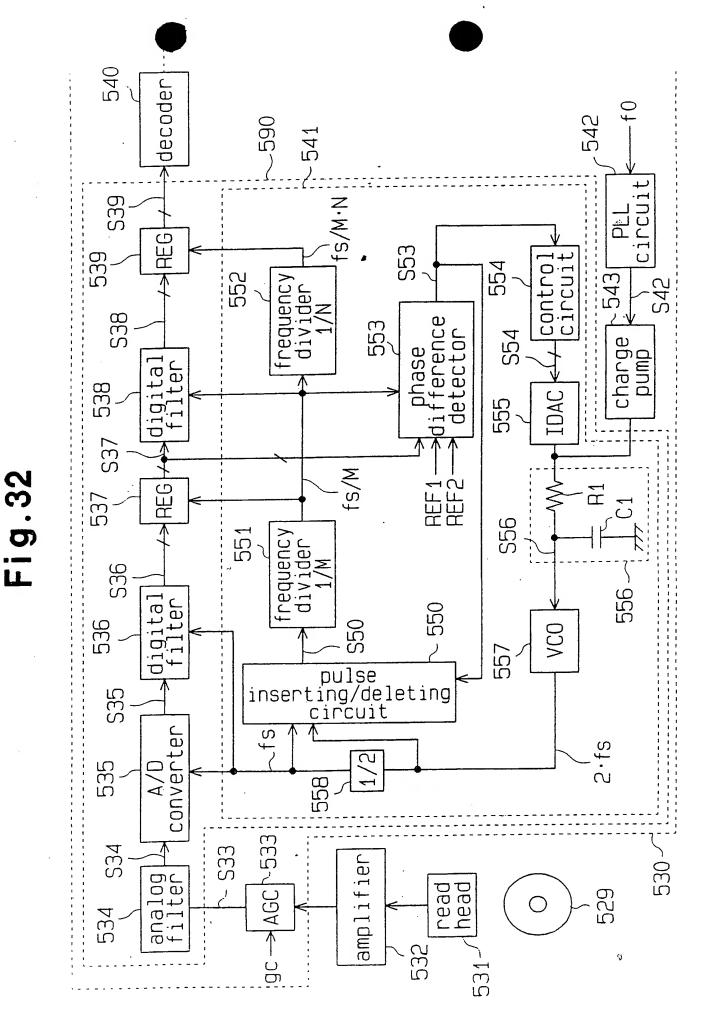
N. 18

Fig. 29



rorear escenor Fig.31





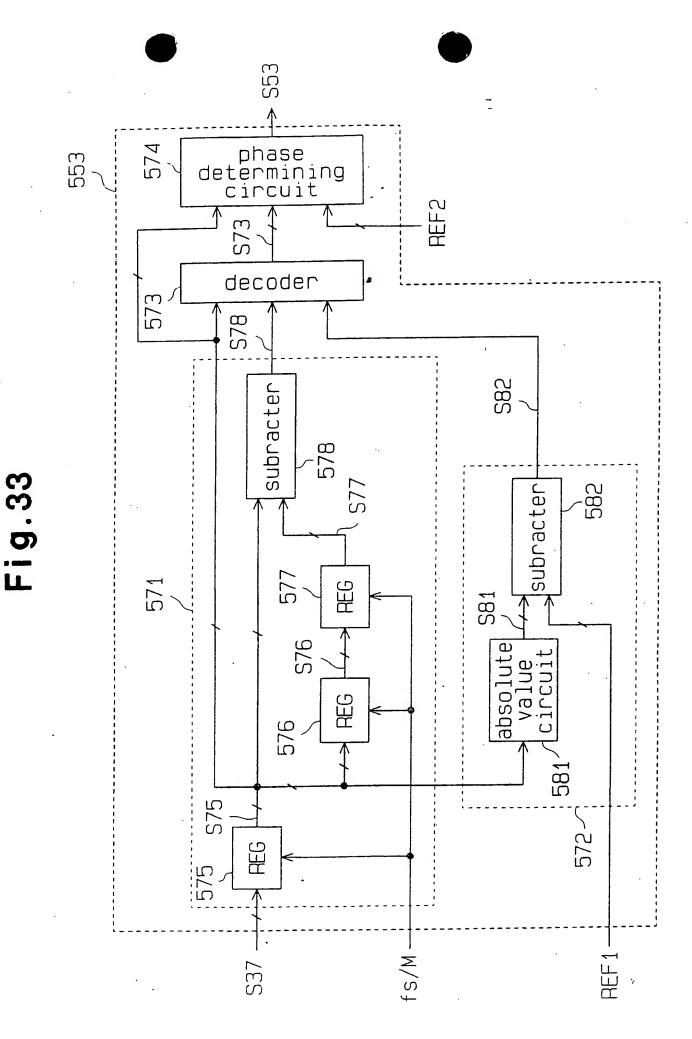


Fig.34A

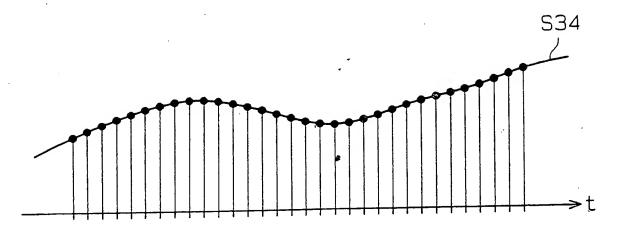


Fig.34B

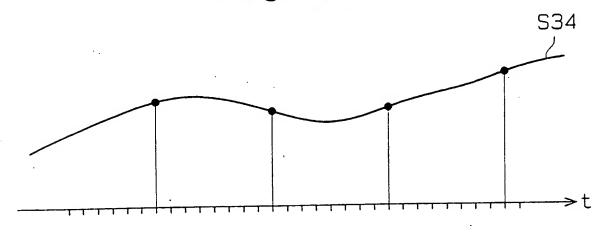


Fig.34C

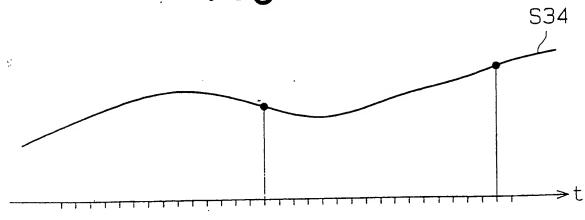


Fig. 35

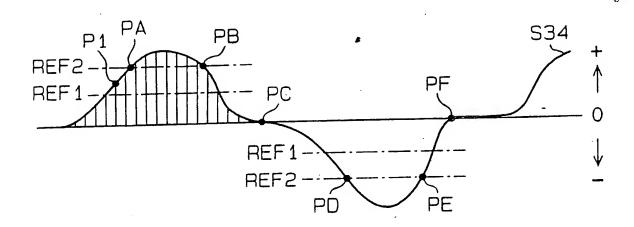


Fig.36

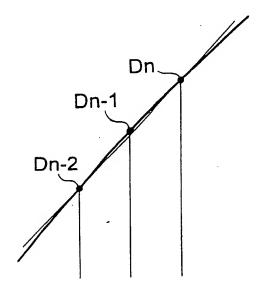


Fig.37

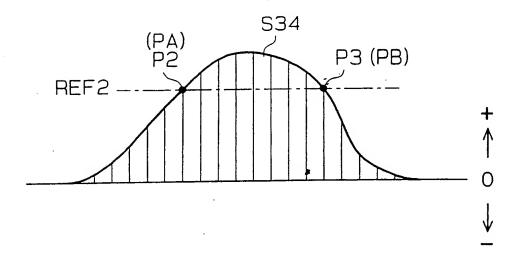


Fig.38

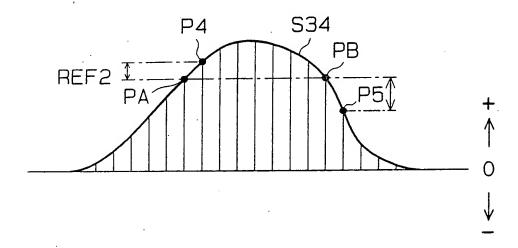


Fig.39

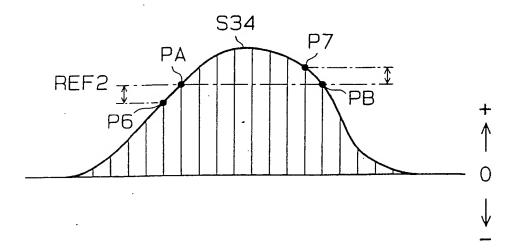


Fig. 40A

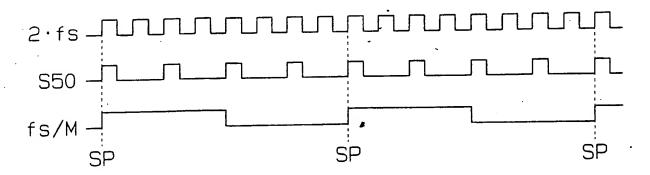


Fig.40B

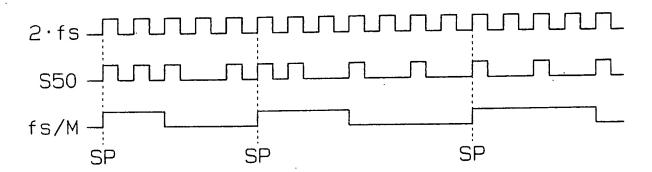
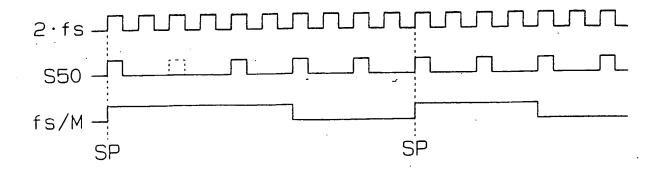


Fig.40C



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